MST66C04D

N & P-Channel 20-V (D-S) MOSFET

Description

The MST66C04D uses advanced trench technology to provide excellent on-resistance and low gate change. The complementary MOSFETs form a high-speed power inverter, suitable for a multitude of applications.
The device meets the RoHS and Green Product requirement with full function reliability approved.

Features

- Advanced high cell density Trench technology
- Low Gate Change
- Low On-resistance
- Green Device Available

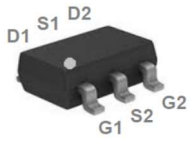
Typical Applications

- Notebook
- Load Switch
- Networking
- Hand-held Instrument

Package type：SOT-26

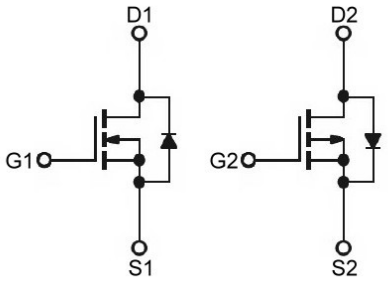
Packing & Order Information

3,000/Reel

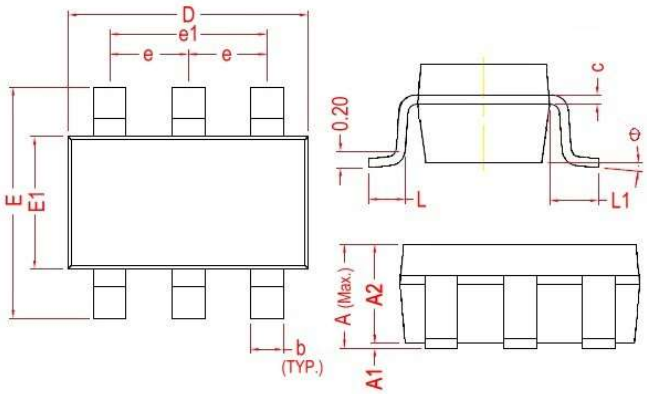


RoHS Compliant

Graphic Symbol

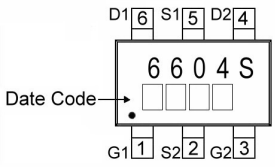


Package Dimension



REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	1.45 Max.		L	0.37 Ref.	
A1	0	0.15	L1	0.60 Ref.	
A2	0.90	1.30	θ	0°	10°
c	0.12 Ref.		b	0.30	0.50
D	2.70	3.10	e	0.95 Ref.	
E	2.60	3.00	e1	1.90 Ref.	
E1	1.40	1.80			

Marking



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MAXIMUM RATINGS AND ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (unless otherwise specified)

Symbol	Parameter	Value		Units
		N-ch	P-ch	
V_{DS}	Drain-Source Voltage	20	-20	V
V_{GS}	Gate-Source Voltage	±10	±10	V
I_D	Continuous Drain Current[1] (T_A =25°C)	3.0	-3.0	A
	Continuous Drain Current[1] (T_A =70°C)	2.4	-2.4	A
I_{DM}	Pulsed Drain Current[2] (T_A =25°C)	13.4	-13.2	A
P_D	Power Dissipation[3] (T_A =25°C)	1.4		W
T_J/T_{STG}	Operating Junction and Storage Temperature	-55 to +150		°C

Thermal Resistance Ratings

Symbol	Parameter	Maximum	Units
$R_{\theta JA}$	Maximum Junction-to-Ambient[1]	90	°C/W

Electrical Characteristics(T_J =25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Ch	Min.	Typ.	Max.	Units
$V_{GS\ (th)}$	Gate Threshold Voltage	V_{DS} =V_{GS}, I_D =250μA V_{DS} =V_{GS}, I_D =-250μA	N P	0.5 -0.5	-	1.2 -1.2	V
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} =0V, I_D =250μA V_{GS} =0V, I_D =-250μA	N P	20 -20	-	-	V
g_{fs}	Forward Transconductance	V_{DS} =5V, I_D =3.0A V_{DS} =-5V, I_D =-2.8A	N P	-	10 7	-	S
I_{GSS}	Gate-Source Leakage Current	V_{DS} =0V, V_{GS} =±10V	N P	-	-	±100	nA
I_{DSS}	Drain-Source Leakage Current	V_{DS} =16V, V_{GS} =0V, T_J =25°C V_{DS} =16V, V_{GS} =0V, T_J =55°C V_{DS} =-16V, V_{GS} =0V, T_J =55°C V_{DS} =-16V, V_{GS} =0V, T_J =55°C	N P	-	-	1 5 -1 -5	μA
$R_{DS\ (on)}$	Static Drain-Source On-Resistance[2]	V_{GS} =4.5V, I_D =3A V_{GS} =2.5V, I_D =2A V_{GS} =1.8V, I_D =1A V_{GS} =-4.5V, I_D =-3A V_{GS} =-2.5V, I_D =-2A V_{GS} =-1.8V, I_D =-1A	N P	-	-	35 45 95 80 120 160	mΩ
V_{SD}	Diode Forward Voltage[2]	I_S =1A, V_{GS} =0V, T_J =25°C I_S =-1A, V_{GS} =0V, T_J =25°C	N P	-	-	1.2 -1.0	V
I_S	Continuous Source Current[14] **(Diode)**	V_G =V_D =0V, Force Current	N P	-	-	3.6 -3.0	A

Notes

1. Surface mounted on 1 in^2 copper pad of FR4 board, t ≤ 5sec; 180℃/W when mounted on minimum copper pad.
2. The data tested by pulsed, pulse width ≤ 300us, duty cycle ≤ 2%.
3. The power dissipation is limited by 150℃ junction temperature.
4. The data is theoretically the same as I_D and I_{DM}, in real applications, should be limited by total power dissipation.

MST66C04D

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Dynamic and switching Characteristics

Symbol	Parameter	Test Conditions	Ch	Min.	Typ.	Max.	Units
Q_g	Total Gate Charge[2]	N-Ch V_{DS} =15V, I_D =3A, V_{GS} =4.5V P-Ch V_{DS} =-10V, I_D =-3A, V_{GS} =-4.5V	N P	-	4.6 4.8	-	nC
Q_{gs}	Gate-Source Charge		N P	-	0.7 0.5	-	
Q_{gd}	Gate-Drain Charge		N P	-	1.5 2.1	-	
$t_{d(on)}$	Turn-On Delay Time[2]	N-Ch V_{DS} =10V, I_D =3A, V_{GS} =4.5V, R_G =3.3Ω P-Ch V_{DS} =-10V, I_D =-1A, V_{GS} =-4.5V R_G =25Ω	N P	-	14 3.6	20 7.0	ns
t_r	Rise Time		N P	-	10.0 12.5	20 25	
$t_{d(off)}$	Turn-Off Delay Time		N P		30.0 32.5	35 65	
t_f	Fall Time		N P	-	7.0 8.5	14 17	
C_{ISS}	Input Capacitance	N-Ch V_{DS} =15V, V_{GS} =0V, f =1.0MHz P-Ch V_{DS} =-15V, V_{GS} =0V, f =1.0MHz	N P	-	396 520	475 615	pF
C_{OSS}	Output Capacitance		N P	-	54 56	-	
C_{RSS}	Reverse Transfer Capacitance		N P	-	40 40	-	

MST66C04D

N & P-Channel 20-V (D-S) MOSFET

- **Typical Electrical Characteristics N-Channel**

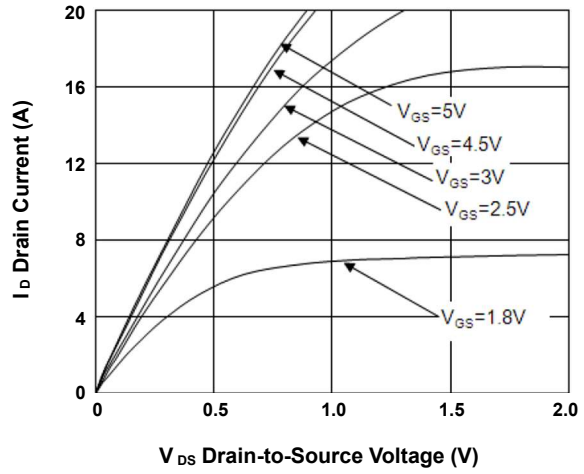

FIG.1-Typical Output Characteristics

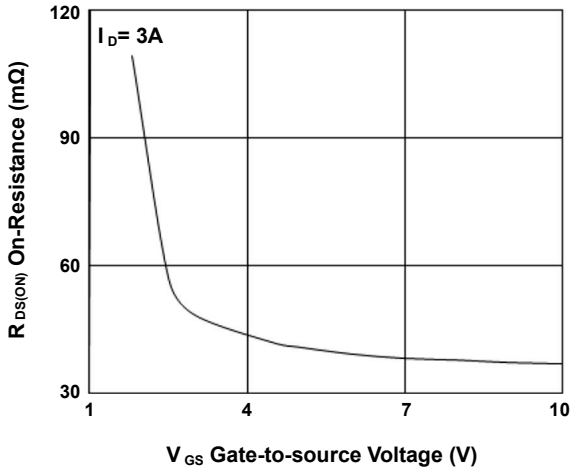

FIG.2-On-Resistance vs. G-S Voltage

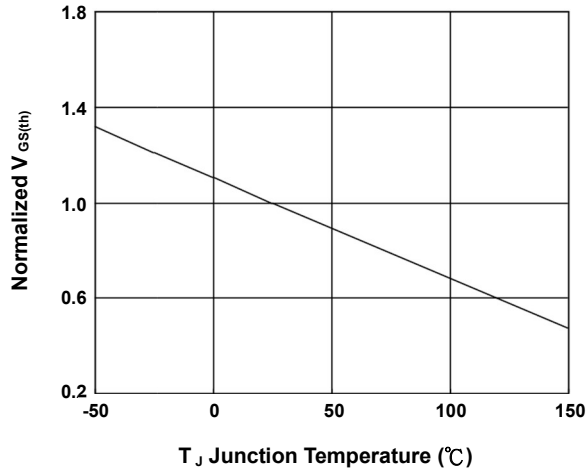

FIG.3-Normalized $V_{GS(th)}$ vs. T_J

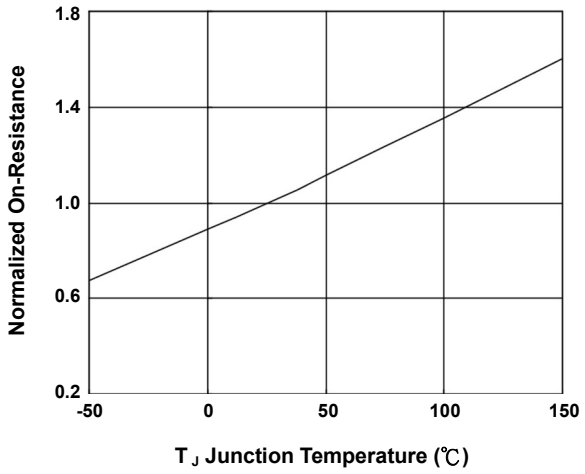

FIG.4-Normalized R_{DSON} vs. T_J

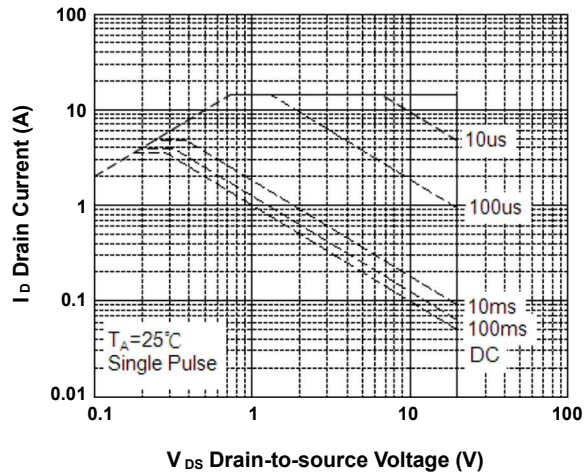

FIG.5-Safe Operating Area

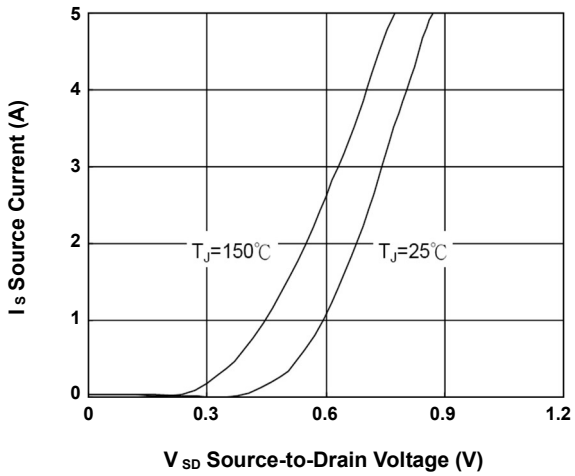

FIG.6-Forward Characteristics of Reverse

MST66C04D

N & P-Channel 20-V (D-S) MOSFET

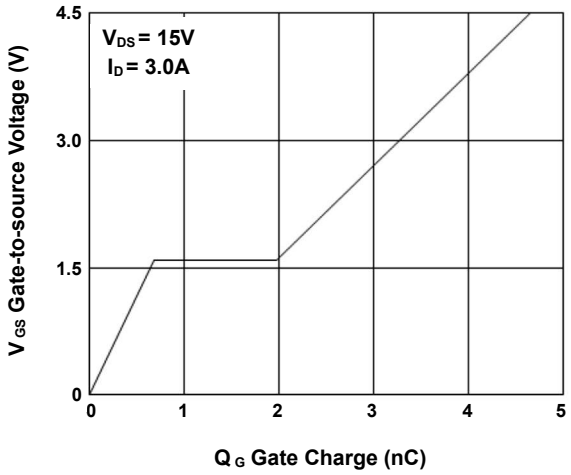

FIG.7-Gate Charge Characteristics

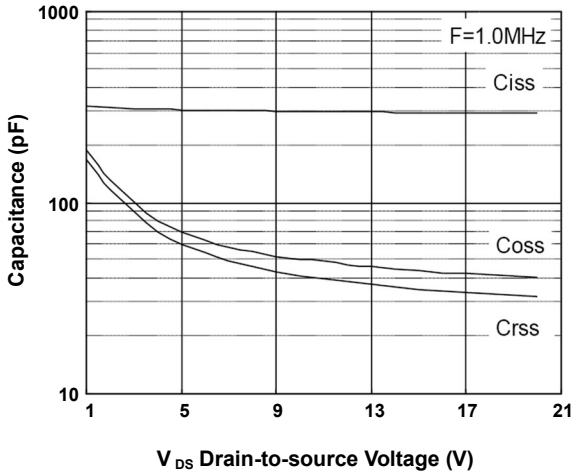

FIG.8-Capacitance Characteristics

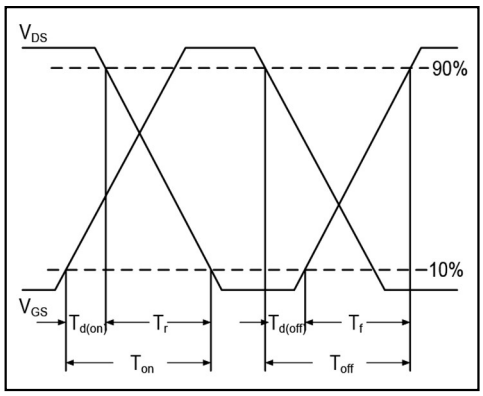

FIG.9-Switching Time Waveform

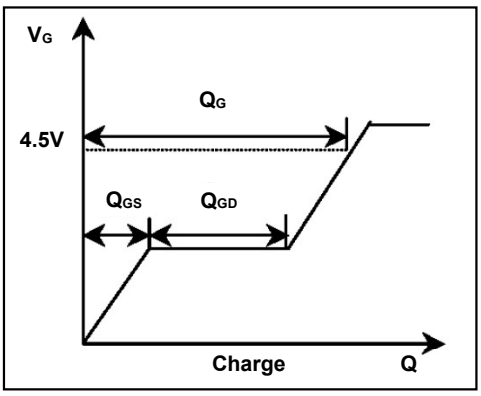

FIG.10-Gate Charge Waveform

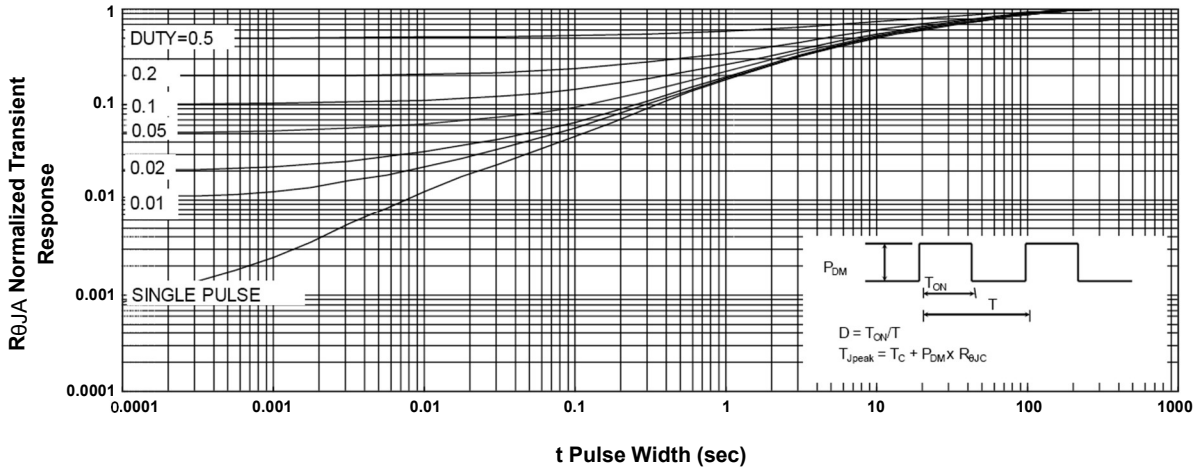

FIG.11-Normalized Maximum Transient Thermal Impedance

MST66C04D

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- **Typical Electrical Characteristics P-Channel**

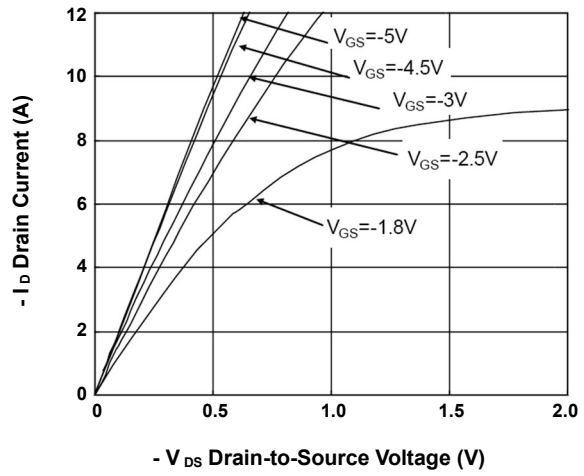
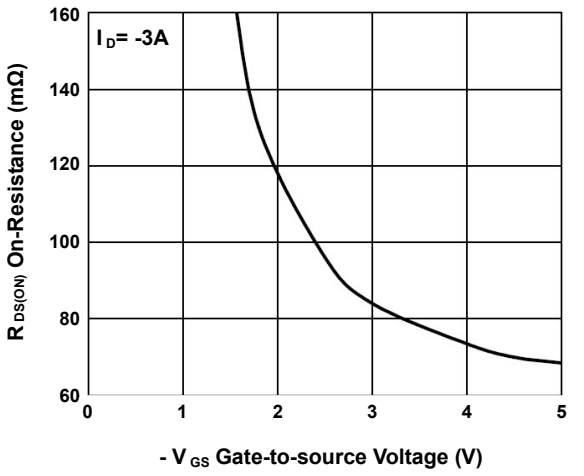


FIG.1-Typical Output Characteristics



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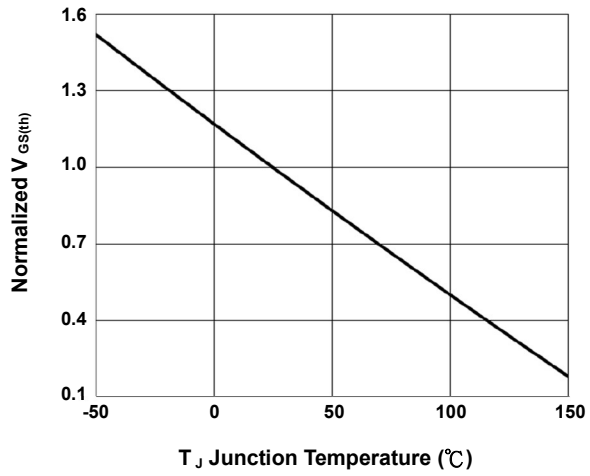

FIG.3-Normalized $V_{GS(th)}$ vs. T_J

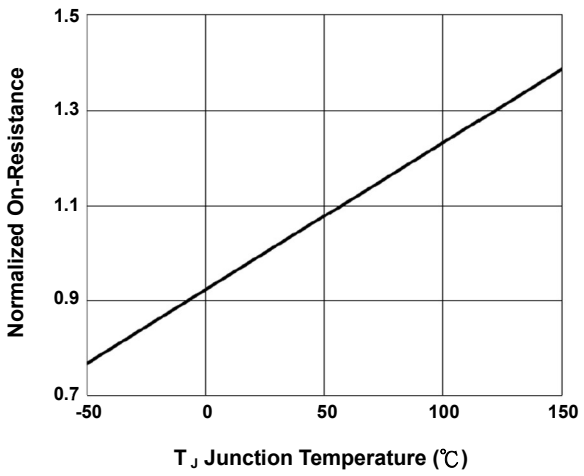

FIG.4-Normalized R_{DSON} vs. T_J

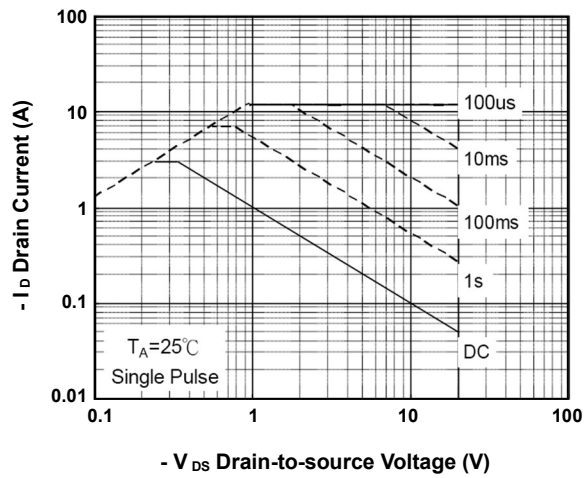

FIG.5-Safe Operating Area

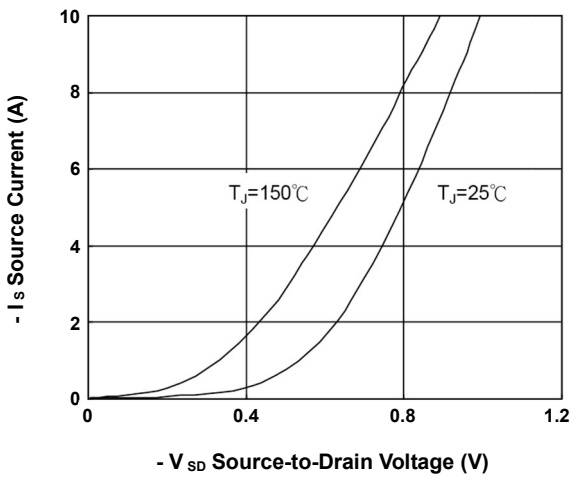

FIG.6-Forward Characteristics of Reverse

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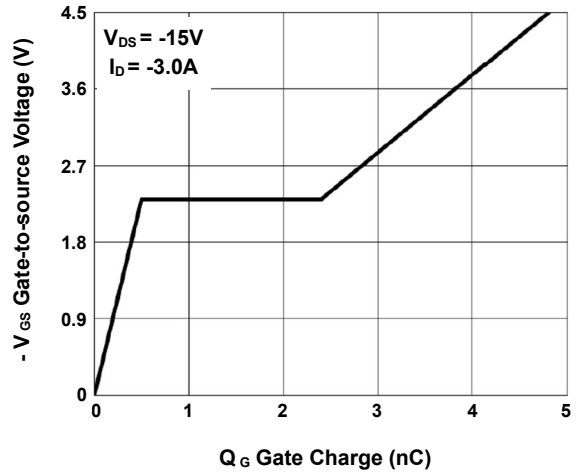


FIG.7-Gate Charge Characteristics

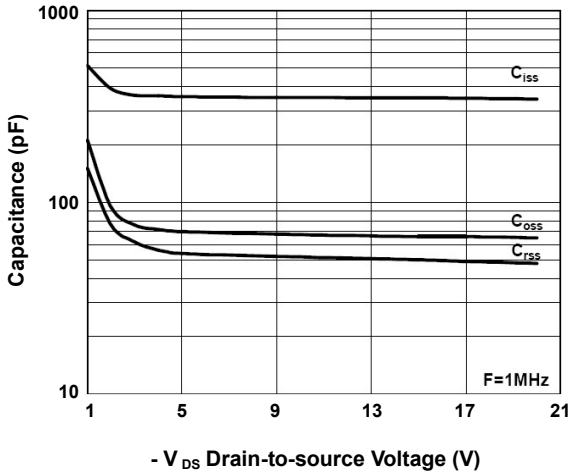
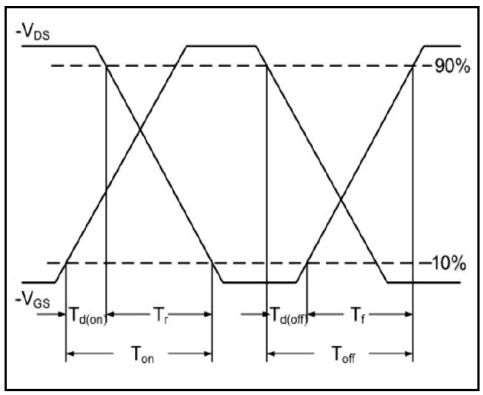


FIG.8-Capacitance Characteristics



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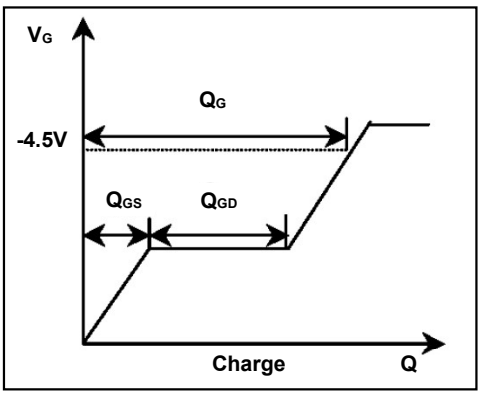

FIG.10-Gate Charge Waveform

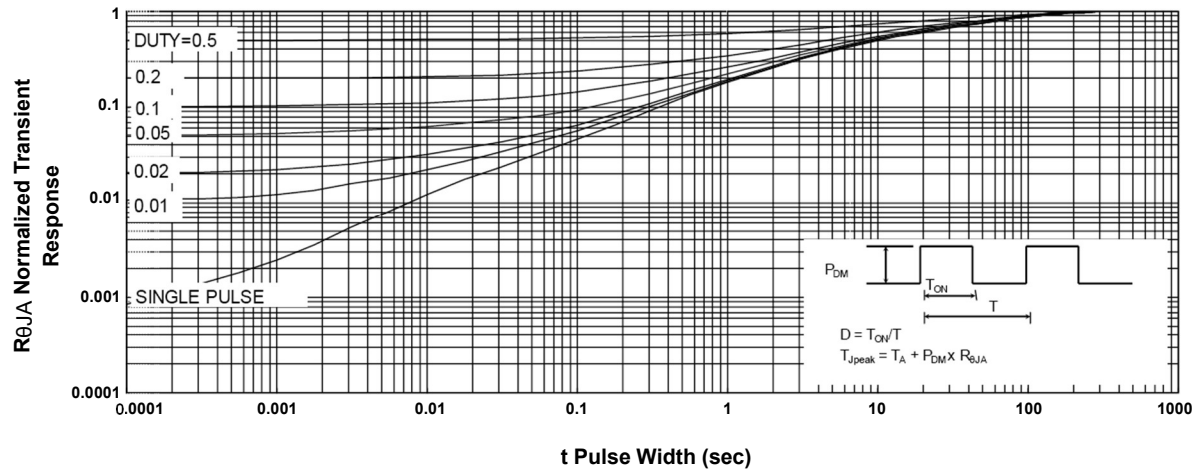

FIG.11-Normalized Maximum Transient Thermal Impedance

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