Brückewell

MSD4N60

600V N-Channel MOSFET

Description

The MSD4N60 is a N-channel enhancement-mode MOSFET , providing the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost effectiveness. The TO-252 package is universally preferred for all commercial-industrial applications

Features

- Low On Resistance
- Simple Drive Requirement
- Low Gate Charge
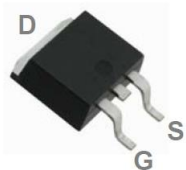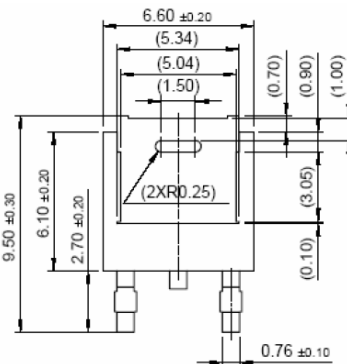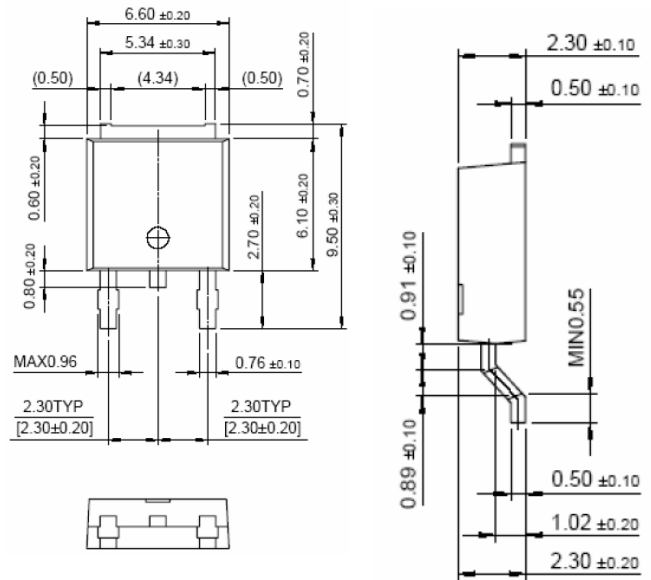- Fast Switching Characteristic
- RoHS compliant package

Application

- Low power battery chargers
- Switch mode power supply (SMPS)
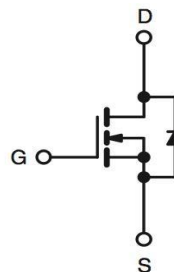- DC-AC converters.

Packing & Order Information

Part No./ R：2,500/Reel

Part No./ T：80/Tube , 4,000/Box

RoHS COMPLIANT

Graphic symbol

MAXIMUM RATINGS AND ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (Tc=25°C unless otherwise noted)			
Symbol	Parameter	Value	Unit
V_{DSS}	Drain-Source Voltage	600	V
V_{GS}	Gate-Source Voltage	±30	V
I_D	Continuous Drain Current (TC=25°C)	4.5	A
	Continuous Drain Current (TC=100°C)	2.6	A
I_{DM}	Pulsed Drain Current	18	A

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Absolute Maximum Ratings (Tc=25°C unless otherwise noted)

Symbol	Parameter	Value	Unit
EAS	Single Pulsed Avalanche Energy	33	mJ
I_{AR}	Avalanche Current	4.0	A
EAR	Repetitive Avalanche Energy	10	mJ
dV/dt	Peak Diode Recovery dV/dt	4.5	V/ns
P_D	Power Dissipation (T_C=25°C)	31	W
	Derating Factor above 25 °C	0.25	W
T_J	Storage Temperature	150	°C
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	°C

Note:

1.Repetitive rating; pulse width limited by maximum junction temperature.

2. I_{AS}=4A, V_{DD}=50V, L=8mH, V_G=10V, starting TJ=+25°C.

3. I_{SD}≤4A, dI/dt≤100A/μs, VDD≤BVDSS, starting TJ=+25°C.

Thermal Resistance Characteristics (Tc=25°C unless otherwise noted)

Symbol	Parameter	Value Min.	Value Typ.	Value Max.	Units
$R_{\theta JC}$	Thermal Resistance,Junction-to-Case	--	--	2.8	°C/W
$R_{\theta JA}$	Thermal Resistance,Junction-to- Ambient	--	--	50	

Off Characteristics

Symbol	Parameter	Test Conditions	Min	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V , I_D=250μA	600	--	--	V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temperature Coefficient	I_D = 250μA, Referenced to 25°C	--	0.60	--	V/°C
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, I_D = 250μA	2.0	--	4.0	V
I_{DSS}	Drain-Source Leakage Current	V_{DS} = 600 V , V_{GS} = 0 V V_{DS} = 480 V , T_C = 125°C	--	--	1 10	uA
I_{GSS}	Gate-Body Leakage Forward	V_{GS} = ±30	--	--	±100	nA
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V , I_D = 2.25 A	--	2.0	2.5	Ω

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Dynamic Characteristics						
Symbol	Parameter	Test Conditions	Min	Typ.	Max.	Units
C_{ISS}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, F = 1.0MHz	--	560	--	pF
C_{OSS}	Output Capacitance		--	55	--	pF
C_{RSS}	Reverse Transfer Capacitance		--	7	--	pF
$t_{d(on)}$	Turn-On Time	V_{DD} = 300 V, I_D = 4.5 A, R_G = 25 Ω , V_{GS} = 10 V	--	10	30	ns
t_r	Turn-On Time		--	40	80	ns
$t_{d(off)}$	Turn-Off Delay Time		--	40	100	ns
tf	Turn-Off Fall Time		--	50	90	ns
Q_g	Total Gate Charge	V_{DD} = 480 V,I_D = 4.5 A, V_{GS} = 10 V	--	16	--	nC
Q_{gs}	Gate-Source Charge		--	2.5	--	nC
Q_{gd}	Gate-Drain Charge		--	6.5	--	nC

Source-Drain Diode						
Symbol	Parameter	Test Conditions	Min	Typ.	Max.	Units
Is		VD = VG = 0	--	--	4.0	A
I_{SM}			--	--	16	
V_{SD}		Is = 4.0 A , V_{GS} = 0 V	--	--	1.4	V
t_{rr}		I_F = 4.0 A , V_{GS} = 0 V diF/dt = 100A/μs	--	270	--	ns
Q_{rr}			--	18	--	uC

*Pulse Test : Pulse Width ≤300μs, Duty Cycle≤2%

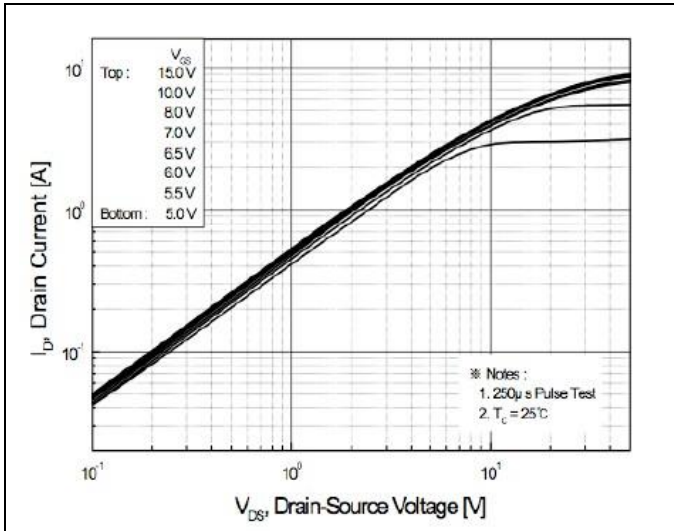■Characteristics Curve

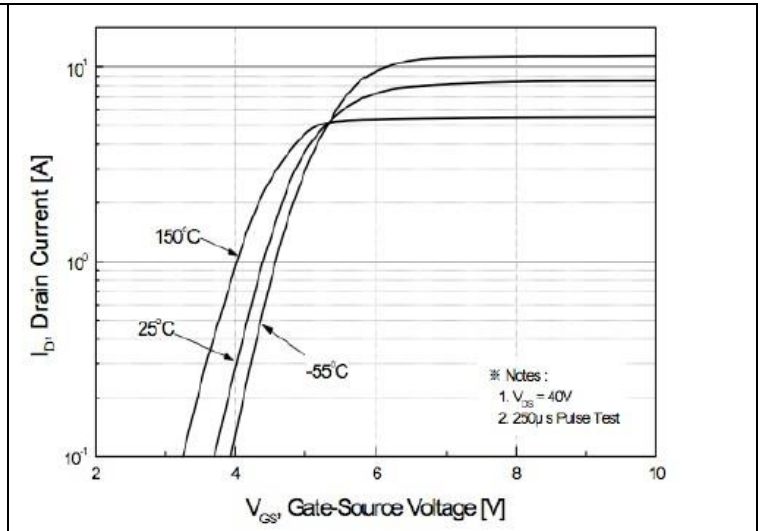FIG.1-ON REGION CHARACTERISTICS

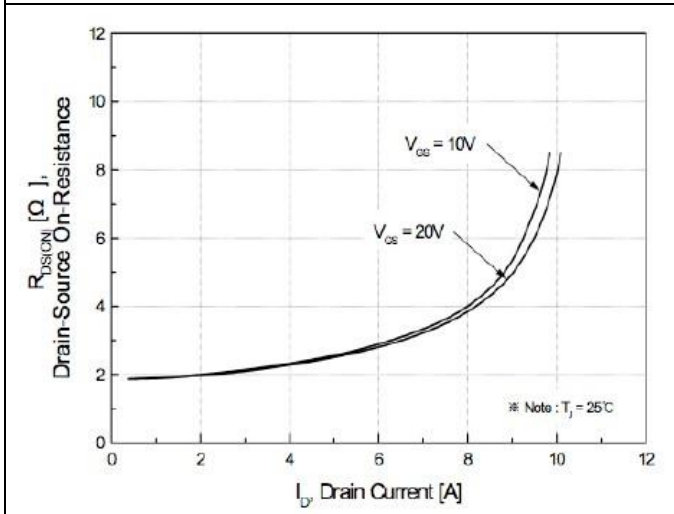
FIG.2-TRANSFER CHARACTERISTICS

FIG.3-ON RESISTANCE VARIATION VS DRAIN
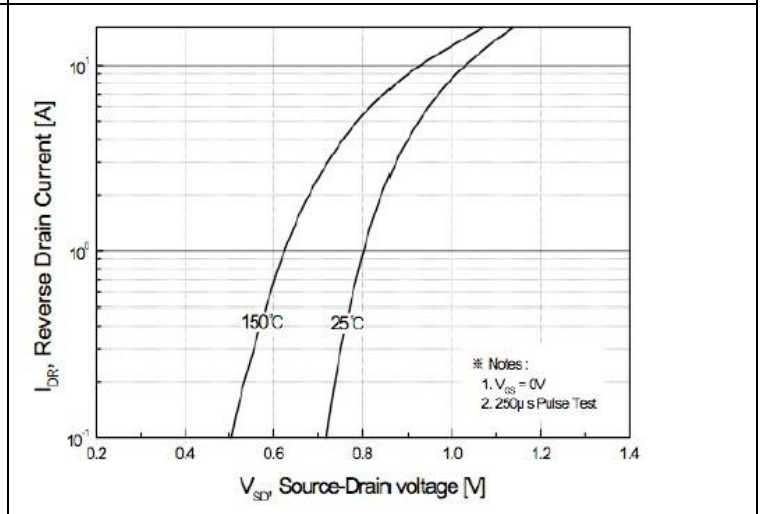CURRENT AND GATE VOLTAGE

FIG.4-BODY DIODE FORWARD VOLTAGE VARIATION
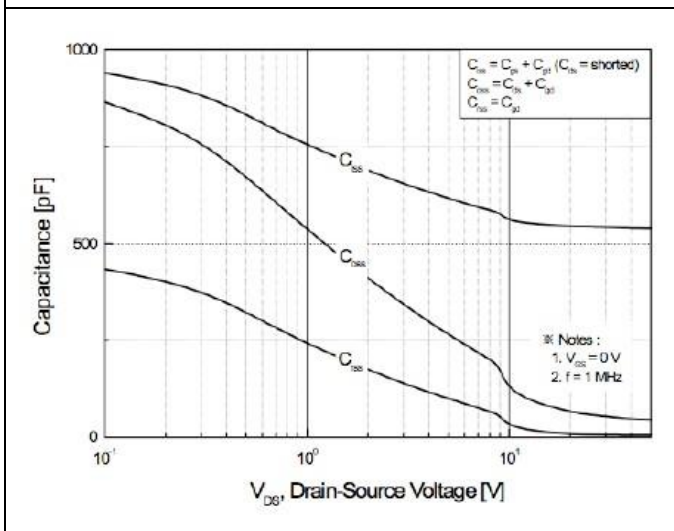WITH SOURCE CURRENT AND TEMPERATURE
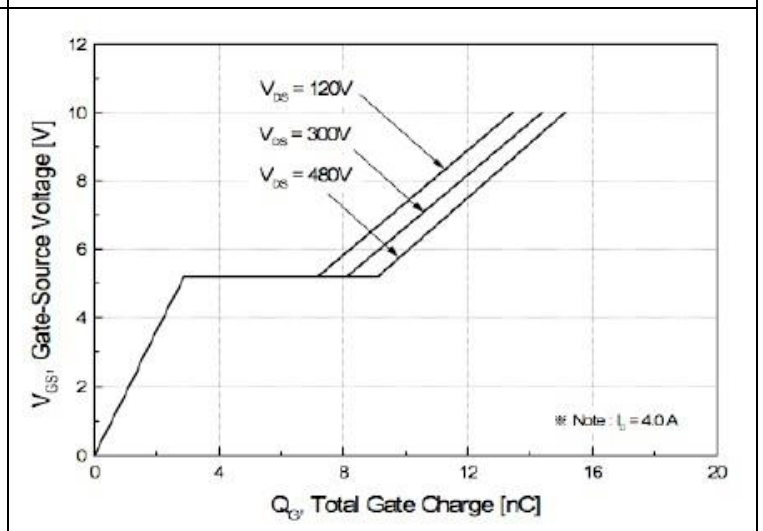

FIG.5-CAPACITANCE CHARACTERISTICS

FIG.6-GATE CHARGE CHARACTERISTICS

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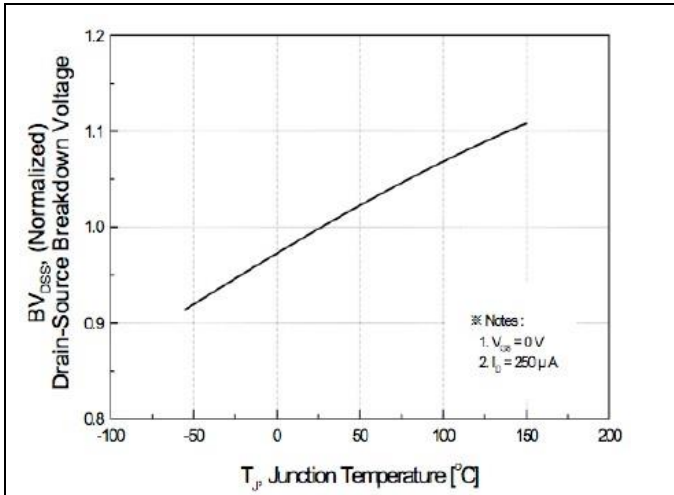## 600V N-Channel MOSFET

■Characteristics Curve

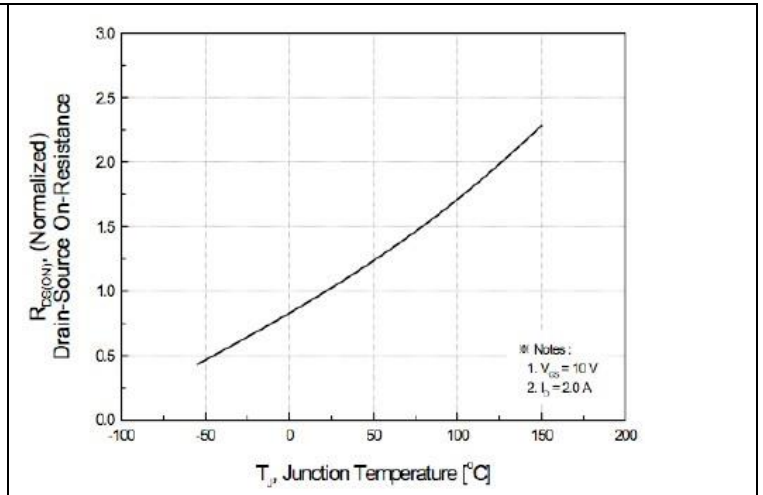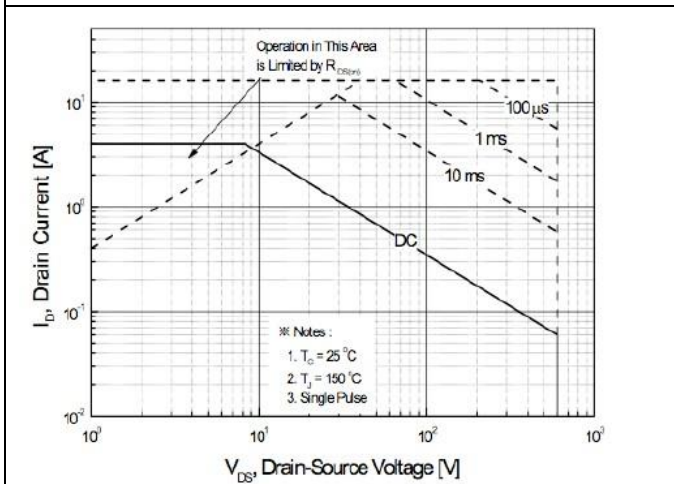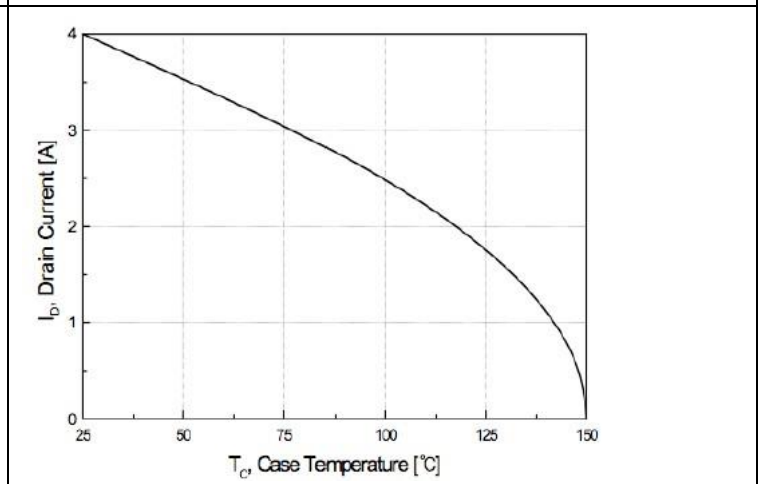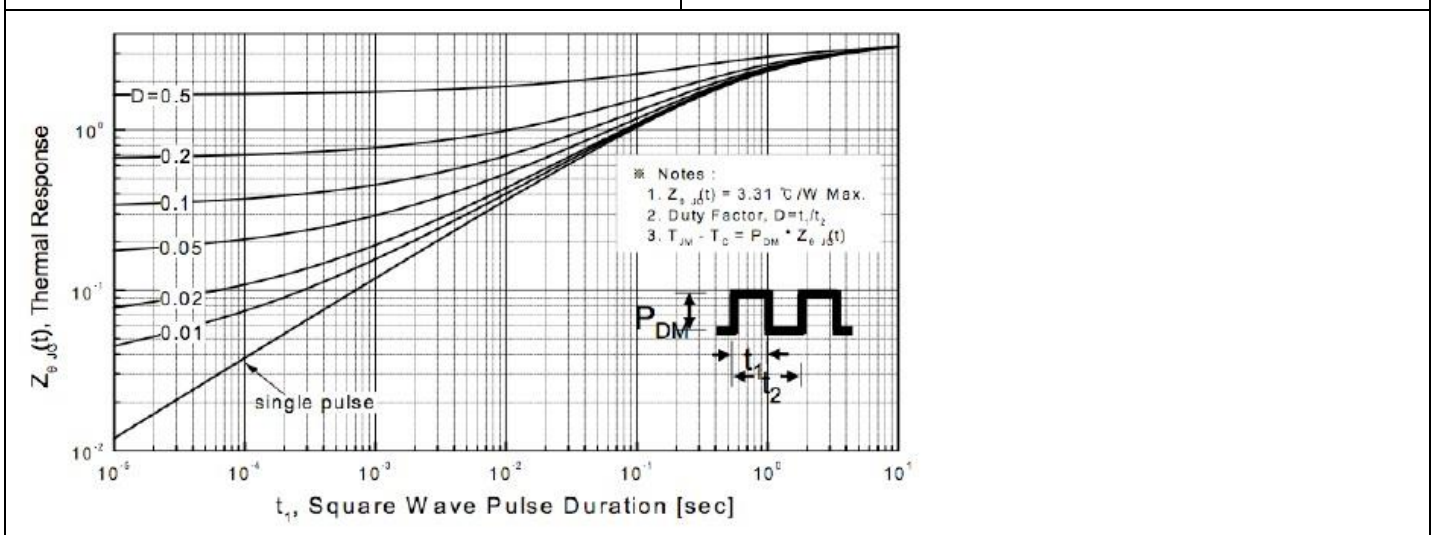|	
FIG.7-BREAKDOWN VOLTAGE VARIATION VS TEMPERATURE	FIG.8-ON-RESISTANCE VARIATION VS TEMPERATURE
FIG.9-MAXIMUM SAFE OPERATING AREA	FIG.10-MAXIMUM DRAIN CURRENT VS CASE TEMPERATURE

FIG.11-TRANSIENT THERMAL RESPONSE CURVE

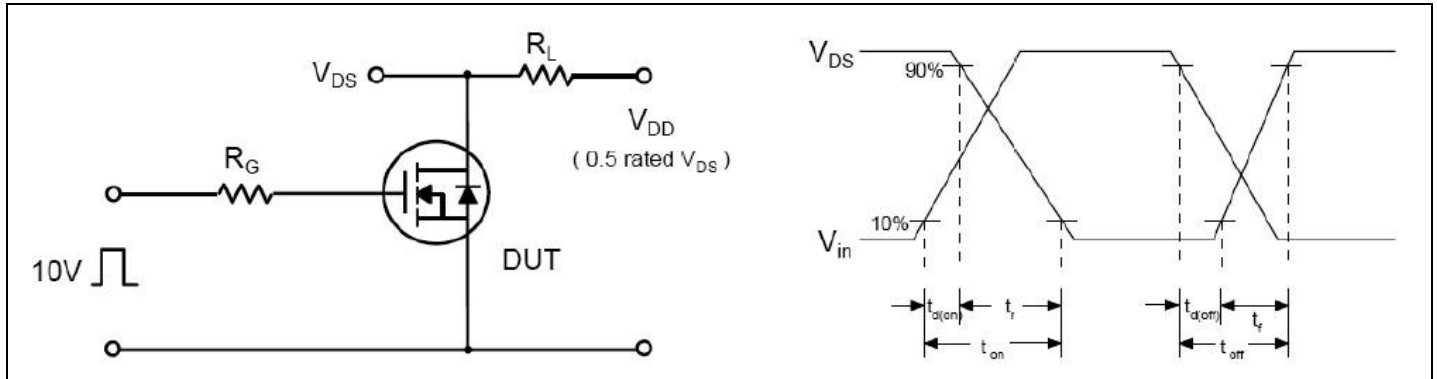## 600V N-Channel MOSFET

■Characteristics Test Circuit & Waveform
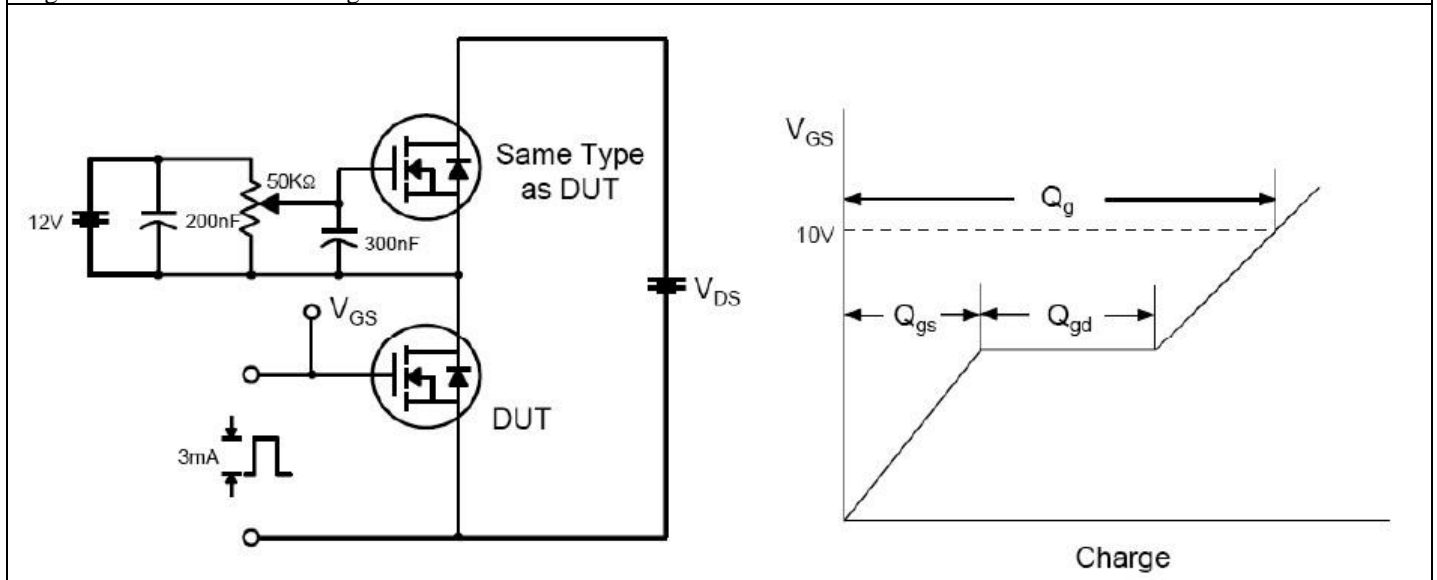

Fig 12. Resistive Switching Test Circuit & Waveforms

Fig 13. Gate Charge Test Circuit & Waveform
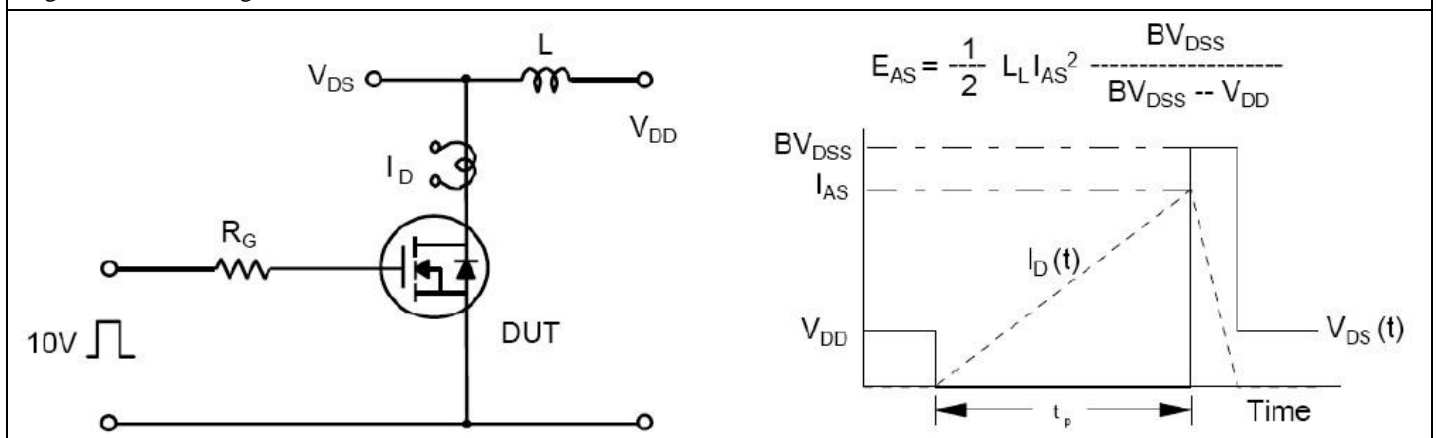

$$E_{AS} = \frac{1}{2} L_L I_{AS}^2 \frac{BV_{DSS}}{BV_{DSS} -- V_{DD}}$$

Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms

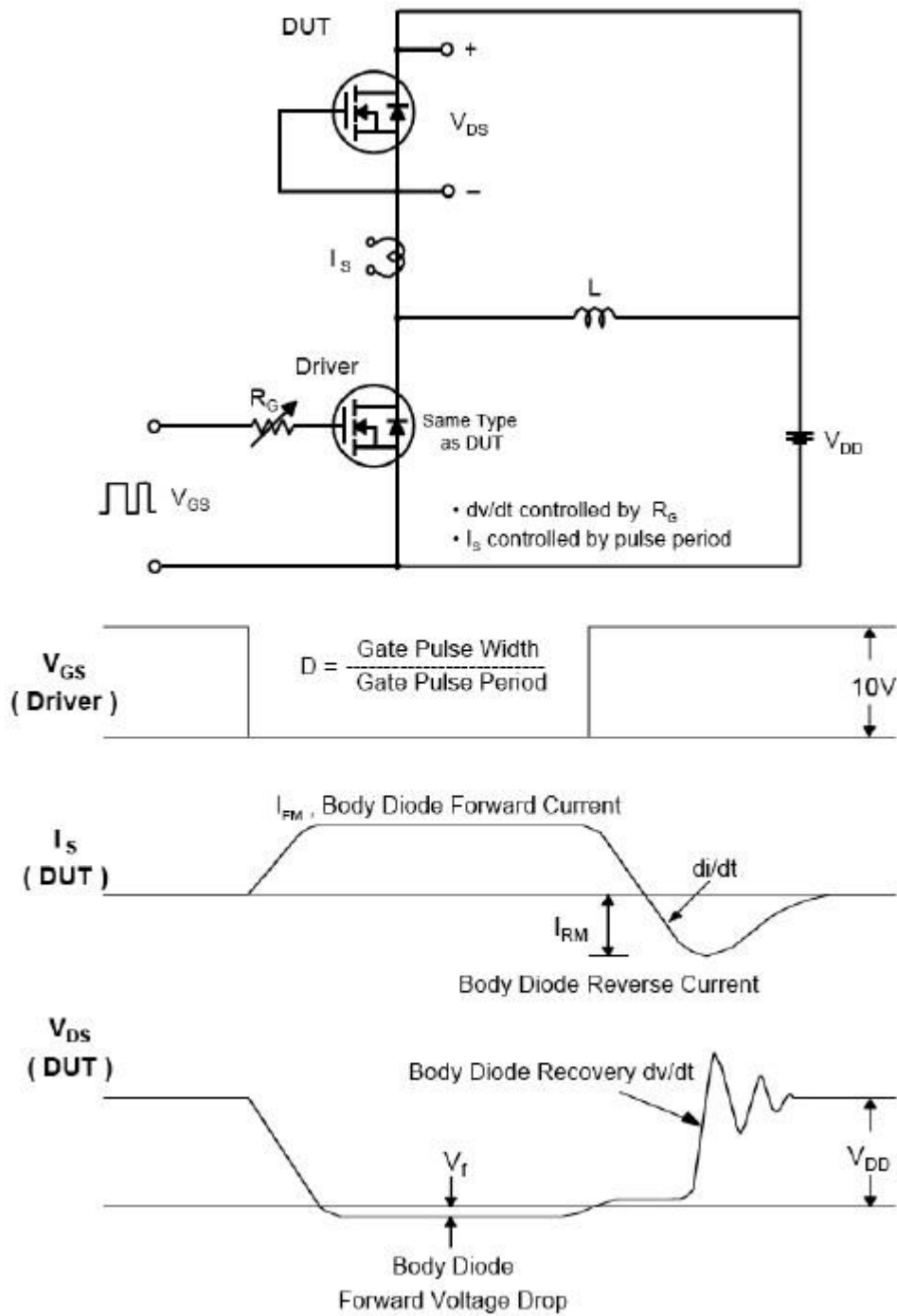## MSD4N60

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Fig 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

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