

MS48N40

N-Channel 40-V (D-S) MOSFET

Description

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $R_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, and PCMCIA cards, cellular and cordless telephones.

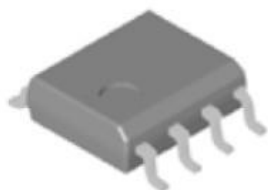
Features

- Low $r_{DS(on)}$ provides higher efficiency and extends battery life
- Miniature SO-8 surface mount package saves board space
- High power and current handling capability
- Low side high current DC-DC Converter applications
- RoHS compliant package

Package type : SO-8

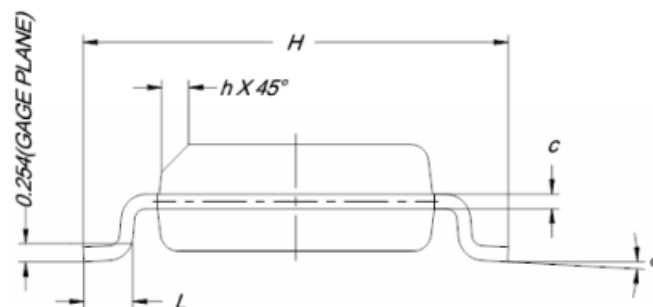
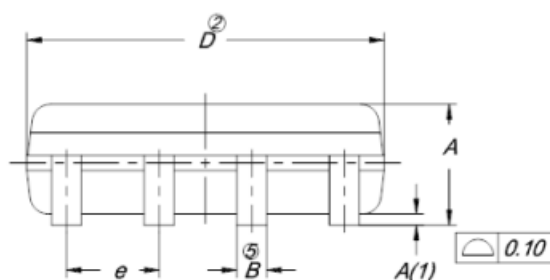
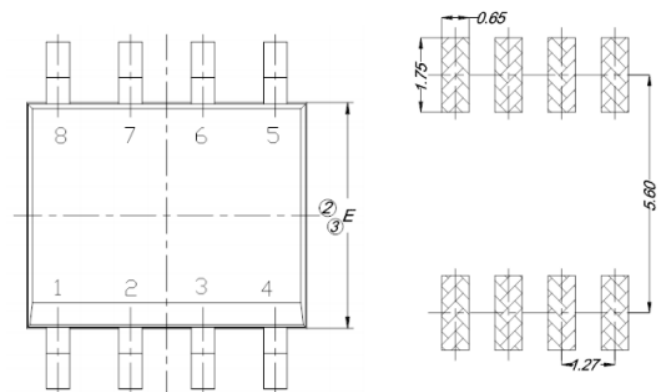
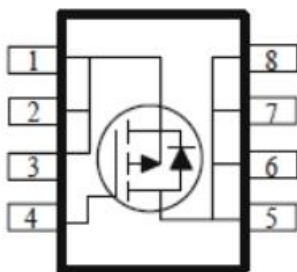
Packing & Order Information

3,000/Reel



**RoHS
COMPLIANT**

Graphic symbol



DIM.	MILLIMETERS		
	MIN.	NOM.	MAX.
A	1.35	1.55	1.75
A(1)	0.10	0.18	0.25
B	0.38	0.45	0.51
C	0.19	0.22	0.25
D	4.80	4.90	5.00
E	3.80	3.90	4.00
e	1.27 BSC		
H	5.80	6.00	6.20
L	0.50	0.72	0.93
α	0°	4°	8°
h	0.25	0.38	0.50

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MAXIMUM RATINGS AND ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Value	Unit
V_{DS}	Drain-Source Voltage	40	V
V_{GS}	Gate-Source Voltage	± 20	V
I_D	Continuous Drain Current ^a ($T_A=25^\circ\text{C}$)	± 9.7	A
	Continuous Drain Current ^a ($T_A=70^\circ\text{C}$)	± 7.2	A
I_{DM}	Pulsed Drain Current ^b	± 50	A
I_S	Continuous Source Current (Diode Conduction) ^a	2.3	A
P_D	Power Dissipation ^a ($T_A=25^\circ\text{C}$)	3.1	W
	Power Dissipation ^a ($T_A=70^\circ\text{C}$)	2.2	W
T_J/T_{STG}	Operating Junction and Storage Temperature	-55 to +150	$^\circ\text{C}$

Thermal Resistance Ratings

Symbol	Parameter	Maximum	Units
$R_{\theta JA}$	Maximum Junction-to-Ambient ^a ($t \leq 10$ sec)	50	$^\circ\text{C/W}$
	Maximum Junction-to-Ambient ^a (Steady-State)	92	

Notes :

- Surface Mounted on 1" x 1" FR4 Board.
- Pulse width limited by maximum junction temperature

Static

Symbol	Parameter	Test Conditions	Min	Typ.	Max.	Units
$V_{GS(th)}$	Gate-Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = -250\mu\text{A}$	1			V
I_{GSS}	Gate-Body Leakage	$V_{DS} = 0$ V, $V_{GS} = 20$ V			± 100	nA
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 24$ V, $V_{GS} = 0$ V $V_{DS} = 24$ V, $V_{GS} = 0$ V, $T_J = 55^\circ\text{C}$			1 25	μA
$I_{D(on)}$	On-State Drain Current	$V_{DS} = 5$ V, $V_{GS} = 10$ V	20			A
$r_{DS(on)}$	Drain-Source On-Resistance	$V_{GS} = 10$ V, $I_D = 9.7$ A $V_{GS} = 4.5$ V, $I_D = 8.8$ A			22 27	m Ω
g_{fs}	Forward Transconductance	$V_{DS} = 15$ V, $I_D = 9.7$ A		40		S
V_{SD}	Diode Forward Voltage	$I_S = 2.3$ A, $V_{GS} = 0$ V		0.7		V

Dynamic^b

Symbol	Parameter	Test Conditions	Min	Typ.	Max.	Units
Q_g	Total Gate Charge	$V_{DS} = 15$ V, $I_D = 9.7$ A, $V_{GS} = 4.5$ V	--	12.5	--	nC
Q_{gs}	Gate-Source Charge		--	2.6	--	nC
Q_{gd}	Gate-Drain Charge		--	4.6	--	nC

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Dynamic ^b						
Symbol	Parameter	Test Conditions	Min	Typ.	Max.	Units
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 25\text{ V}, R_L = 25\ \Omega,$ $V_{GEN} = 10\text{ V}, I_D = 1\text{ A}$	--	20	--	ns
t_r	Rise Time		--	9	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	70	--	ns
t_f	Fall Time		--	20	--	ns

Notes :

a. Pulse test: $PW \leq 300\mu s$ duty cycle $\leq 2\%$.

b. Guaranteed by design, not subject to production testing.

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