

MS34N34

Dual N-Channel 20-V (D-S) MOSFET

Description

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low rDS(on) and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

Features

- Low rDS(on) provides higher efficiency and
- extends battery life
- Low thermal impedance copper lead frame

RoHS COMPLIANT

TSOP-6 saves board space

- Fast switching speed
- High performance trench technology
- RoHS compliant package

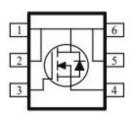
Package type : TSOP-6

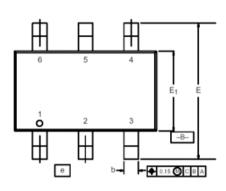
Packing & Order Information

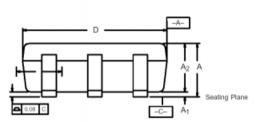
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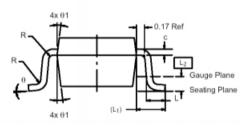


Graphic symbol









	MIL	LIMET	ERS	INCHES			
Dim	Min	Nom	Max	Min	Nom	Max	
Α	0.91	-	1.10	0.036	-	0.043	
A ₁	0.01	-	0.10	0.0004	-	0.004	
A ₂	0.84	-	1.00	0.033	0.038	0.039	
b	0.30	0.32	0.45	0.012	0.013 0.01		
с	0.10	0.15	0.20	0.004	0.006	0.008	
D	2.95	3.05	3.10	0.116	0.120	0.122	
E	2.70	2.85	2.98	0.106	0.112	0.117	
E ₁	1.55	1.65	1.70	0.061	0.065	0.067	
е	1.00 BSC			0.0394 BSC			
L	0.35	-	0.50	0.014	- 0.020		
L ₁	0.60 Ref			0.024 Ref			
L ₂	0.25 BSC			0.010 BSC			
R	0.10	-	-	0.004	-	-	
θ	0°	4°	8°	0°	4°	8°	
θ1		7° Nom			7° Nom		



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Absolute Maximum Ratings (Tc=25°C unless otherwise specified)					
Symbol	Parameter	Value	Unit		
V _{DS}	Drain-Source Voltage	30	V		
V _{GS}	Gate-Source Voltage	±12	V		
ID	Continuous Drain Current ^a (T _A =25°C)	6.0	А		
	Continuous Drain Current ^a (T _A =70°C)	4.6	А		
IDM	Pulsed Drain Current ^b	±20	А		
Is	Continuous Source Current (Diode Conduction) ^a	1.6	А		
P _D	Power Dissipation ^a ($T_A = 25^{\circ}C$)	2.0	W		
	Power Dissipation ^a ($T_A = 70^{\circ}C$)	1.3	W		
Tj/Tstg	Operating Junction and Storage Temperature	-55 to +150	°C		

Thermal Resistance Ratings						
Symbol	Parameter Maximum Units					
Rthja	Maximum Junction-to-Ambient ^a (t <= 5 sec)	62.5	°C/W			
	Maximum Junction-to-Ambient ^a (Steady-State)	110	C/ W			

Notes:

a. Surface Mounted on 1" x 1" FR4 Board.

b. Pulse width limited by maximum junction temperature

Static						
Symbol	Parameter	Test Conditions	Min	Typ.	Max.	Units
$V_{GS(th)}$	Gate-Threshold Voltage	$V_{DS}=V_{GS},\ I_{D}=-250\mu A$	0.7		15	V
I _{GSS}	Gate-Body Leakage	$V_{DS} = 0 V$, $V_{GS} = \pm 8 V$			±100	nA
Idss	Zero Gate Voltage Drain Current				1 10	uA
I _{D(on)}	On-State Drain Current ^A	$V_{DS} = 5 V, V_{GS} = 4.5 V$	10			А
R _{DS(on)}	Drain-Source On-Resistance ^A	$V_{GS} = 4.5 V, I_D = 6.0 A$ $V_{GS} = 2.5 V, I_D = 5.0 A$			32 44	mΩ
g _{fs}	Forward Tranconductance ^A	$V_{DS} = 10 \text{ V}, I_D = 4.0 \text{ A}$		11.3		S
Vsd	Diode Forward Voltage	$I_S = 1.6 \text{ A}, V_{GS} = 0 \text{ V}$		0.75		V

Dynamic ^b							
Symbol	Parameter	Test Conditions	Min	Typ.	Max.	Units	
t _{d(on)}	Turn-On Delay Time	$V_{DD} = 10 \text{ V}, \text{ R}_{L} = 15 \Omega,$		8		ns	
tr	Rise Time			24		ns	
td(off)	Turn-Off De la y Time	$V_{GEN} = 4.5 V$, $I_D = 5 A$		35		ns	
t _f	Fall Time			10		ns	



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Dynamic ^b								
Symbol	Parameter	Test Conditions	Min	Typ.	Max.	Units		
\mathbf{Q}_{g}	Total Gate Charge	$V_{DS} = 10 \text{ V}, \text{ I}_{D} = 4.0 \text{ A},$ $V_{GS} = 4.5 \text{ V}$		60		nC		
Q_{gs}	Gate-Source Charge			1.0		nC		
Q_{gd}	Gate-Drain Charge			1.5		nC		

Notes:

a. Pulse test: PW <= 300us duty cycle <= 2%.

b. Guaranteed by design, not subject to production testing.



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