

MS34N00

N-Channel 30-V (D-S) MOSFET

Description

The MS34N00 is the highest performance trench N-ch MOSFETs with extreme high cell density, which provide excellent $R_{DS(ON)}$ and gate charge for most of the small power switching and load switch applications.

The device meets the RoHS and Green Product requirement with full function reliability approved.

Features

- Advanced high cell density Trench technology
- Super Low Gate Charge
- Excellent CdV/dt effect decline
- Green Device Available

Typical Applications

- Battery Protection
- Load Switch
- Hand-held Instrument

Package type : SOT-23

AEC-Q101 qualified available

- Automotive ordering code: base /H3

Packing & Order Information

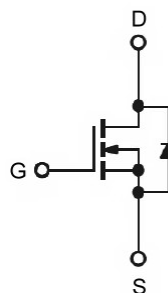
3,000/Reel



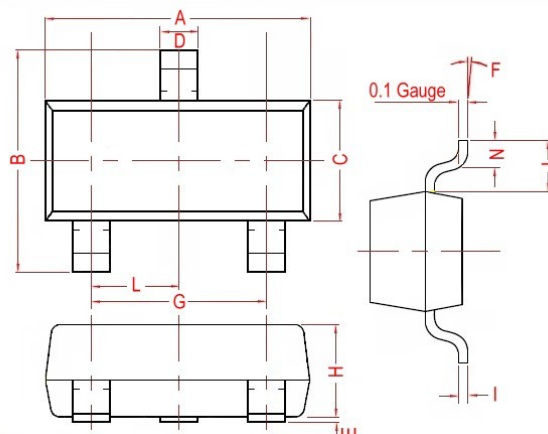
AEC-Q101 Qualified
Available

RoHS Compliant

Graphic Symbol

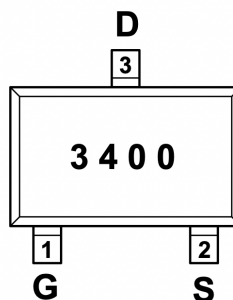


Package Dimension



REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	2.70	3.10	G	1.90 Ref.	
B	2.30	3.00	H	0.90	1.30
C	1.20	1.75	I	0.05	0.21
D	0.30	0.50	J	0.58 Ref.	
E	0.01	0.15	L	0.95 Typ.	
F	0°	10°	N	0.20 Min.	

Marking



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MAXIMUM RATINGS AND ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (unless otherwise specified)			
Symbol	Parameter	Value	Units
V_{DS}	Drain-Source Voltage	30	V
V_{GS}	Gate-Source Voltage	± 12	V
I_D	Continuous Drain Current ($T_A = 25^\circ\text{C}$)	5.8	A
	Continuous Drain Current ($T_A = 70^\circ\text{C}$)	4.9	A
I_{DM}	Pulsed Drain Current ² ($T_A = 25^\circ\text{C}$)	23	A
P_D	Power Dissipation ³ ($T_A = 25^\circ\text{C}$)	1	W
T_J/T_{STG}	Operating Junction and Storage Temperature	-55 to +150	$^\circ\text{C}$

Thermal Resistance Ratings			
Symbol	Parameter	Maximum	Units
$R_{\theta JA}$	Maximum Junction-to-Ambient ¹	125	$^\circ\text{C/W}$
$R_{\theta JA}$	Maximum Junction-to-Ambient ¹ ($t \leq 10\text{s}$)	85	$^\circ\text{C/W}$

Electrical Characteristics($T_J = 25^\circ\text{C}$ unless otherwise specified)						
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 250\mu\text{A}$	0.5	-	1.5	V
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{V}$, $I_D = 250\mu\text{A}$	30	-	-	V
g_{fs}	Forward Transconductance	$V_{DS} = 5\text{V}$, $I_D = 5\text{A}$	-	25	-	S
I_{GSS}	Gate-Source Leakage Current	$V_{DS} = 0\text{V}$, $V_{GS} = \pm 12\text{V}$	-	-	± 100	nA
I_{DSS}	Drain-Source Leakage Current	$V_{DS} = 24\text{V}$, $V_{GS} = 0\text{V}$, $T_J = 25^\circ\text{C}$	-	-	1	μA
		$V_{DS} = 24\text{V}$, $V_{GS} = 0\text{V}$, $T_J = 55^\circ\text{C}$	-	-	5	μA
$R_{DS(on)}$	Static Drain-Source On-Resistance ²	$V_{GS} = 10\text{V}$, $I_D = 5.0\text{A}$	-	-	26	m Ω
		$V_{GS} = 4.5\text{V}$, $I_D = 5.0\text{A}$	-	-	30	
		$V_{GS} = 2.5\text{V}$, $I_D = 2.6\text{A}$	-	-	45	
V_{SD}	Diode Forward Voltage ²	$I_S = 1.2\text{A}$, $V_{GS} = 0\text{V}$, $T_J = 25^\circ\text{C}$	-	-	1.2	V
I_S	Continuous Source Current ^{1,4} (Diode)	$V_G = V_D = 0\text{V}$, Force Current	-	-	5.8	A

Notes

1. Surface mounted on a 1 inch² FR-4 board with 20Z copper.
2. The data tested by pulsed, pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$.
3. The power dissipation is limited by 150°C junction temperature.
4. The data is theoretically the same as I_D and I_{DM} , in real applications, should be limited by total power dissipation.

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Dynamic and switching Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
Q_g	Total Gate Charge	$V_{DS}=15V$	--	11.5	--	nC
Q_{gs}	Gate-Source Charge	$I_D=5.8A$	--	1.6	--	
Q_{gd}	Gate-Drain Charge	$V_{GS}=4.5V$	--	2.9	--	
$t_{d(on)}$	Turn-On Delay Time	$V_{DS}=15V$	--	5	--	ns
t_r	Rise Time	$I_D=5A$	--	47	--	
$t_{d(off)}$	Turn-Off Delay Time	$V_{GS}=10V$	--	26	--	
t_f	Fall Time	$R_G=3\Omega$	--	8	--	
C_{iss}	Input Capacitance	$V_{DS}=15V$	--	860	--	pF
C_{oss}	Output Capacitance	$V_{GS}=0V$	--	84	--	
C_{rss}	Reverse Transfer Capacitance	$f=1.0MHz$	--	70	--	

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- Typical Electrical Characteristics

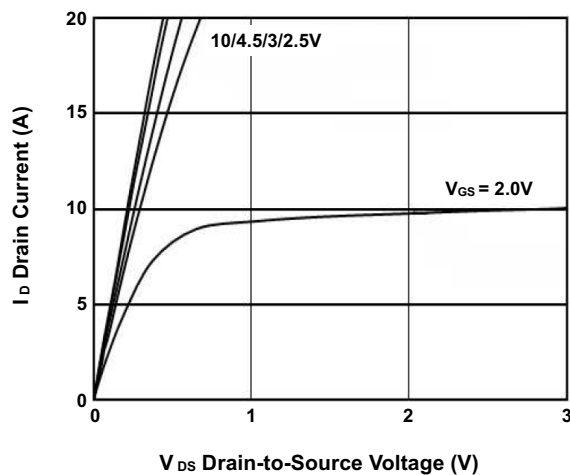


FIG.1-Typical Output Characteristics

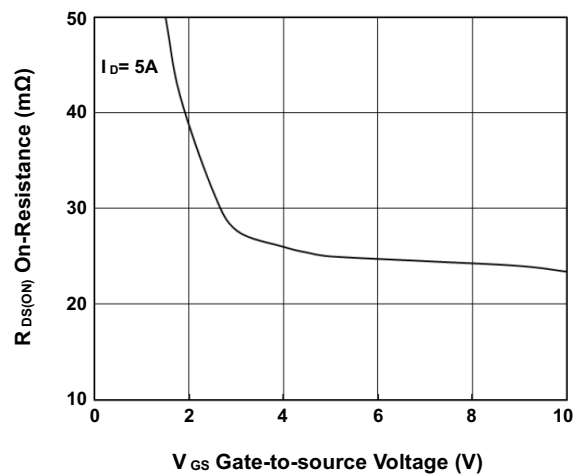


FIG.2-On-Resistance vs. G-S Voltage

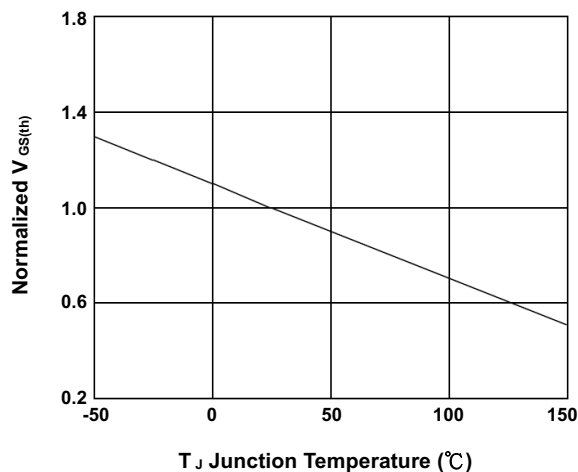


FIG.3-Normalized $V_{GS(th)}$ vs. T_J

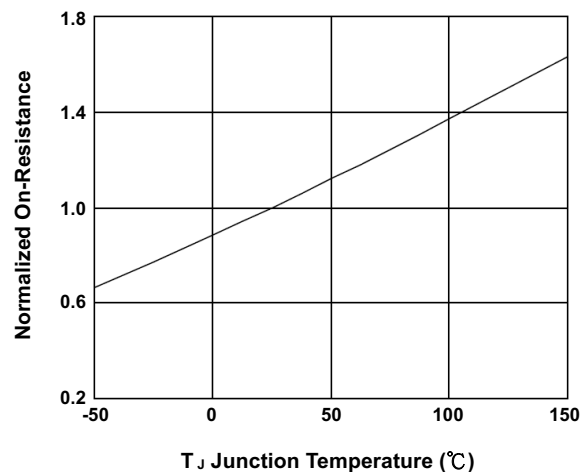


FIG.4-Normalized $R_{DS(on)}$ vs. T_J

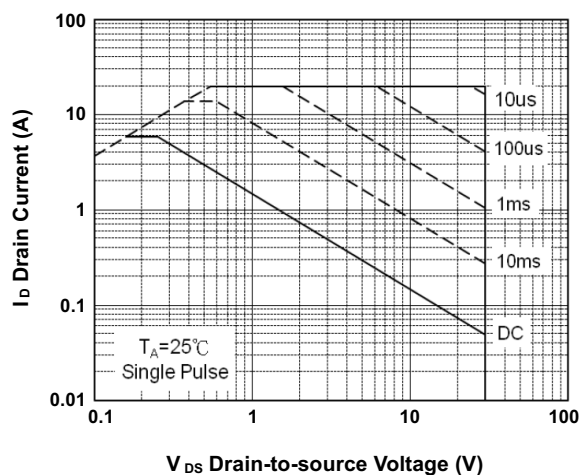


FIG.5-Safe Operating Area

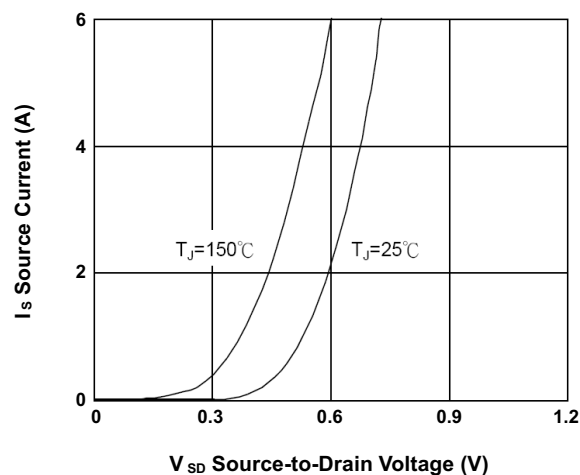


FIG.6-Forward Characteristics of Reverse

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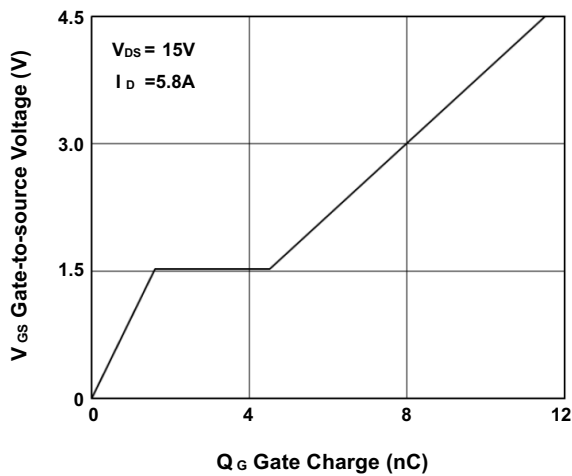


FIG.7-Gate Charge Characteristics

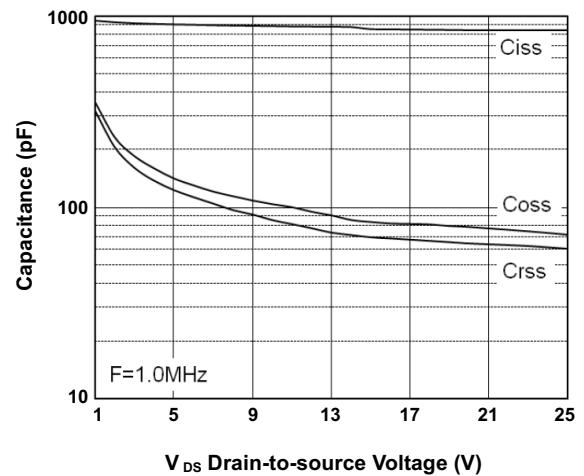


FIG.8-Capacitance Characteristics

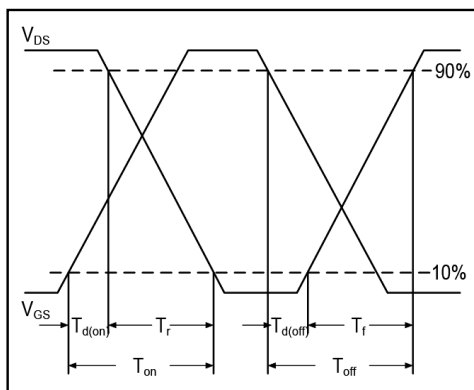


FIG.9-Switching Time Waveform

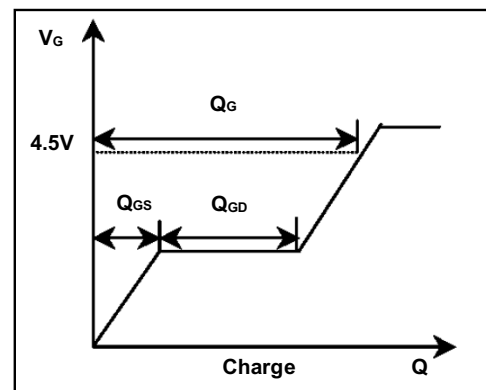


FIG.10-Gate Charge Waveform

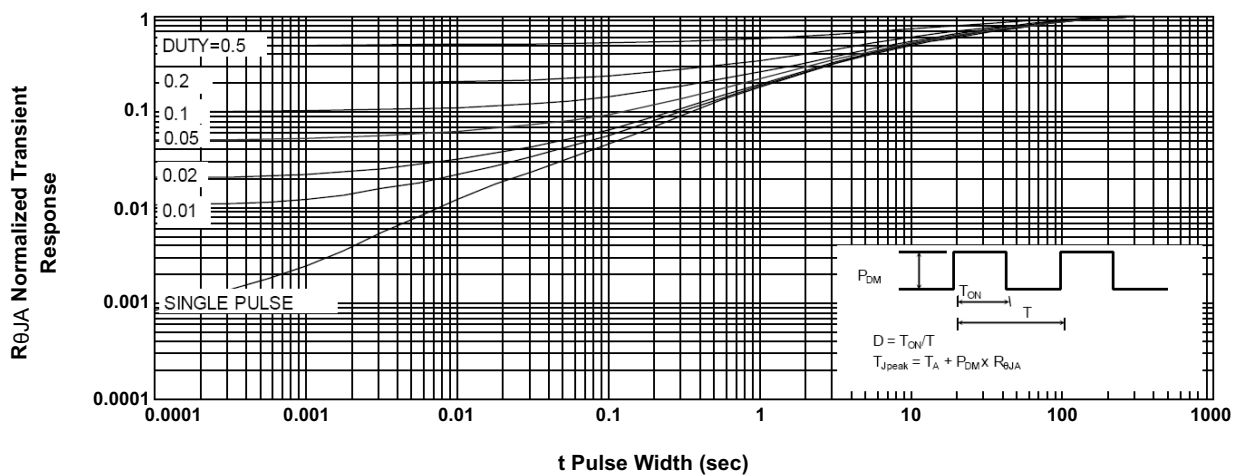


FIG.11-Normalized Maximum Transient Thermal Impedance

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