# MS15P03

**P-CHANNEL ENHANCEMENT MODE POWER MOSFET**

| | |
|---|---|
| $BV_{DSS}$ | -30V |
| $R_{DS(ON)}$ | 12mΩ |
| $I_D$ | -15A |

## Description

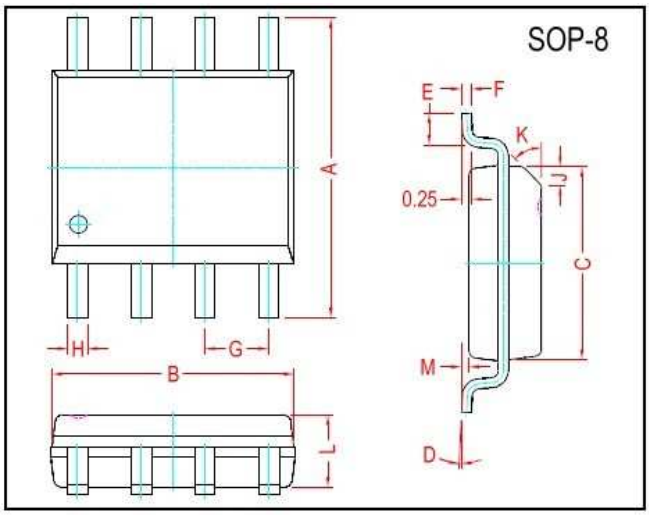
The MS15P03 is the highest performance trench P-ch MOSFETs with extreme high cell density, which provide excellent $R_{DS(ON)}$ and gate charge for most of the synchronous buck converter applications.

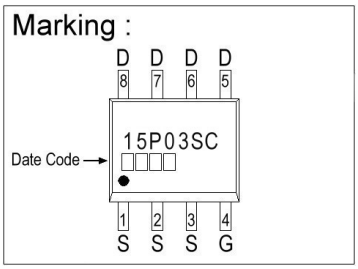
The MS5P03 meet the RoHS and Green Product requirement, 100% EAS guaranteed with full function reliability approved.

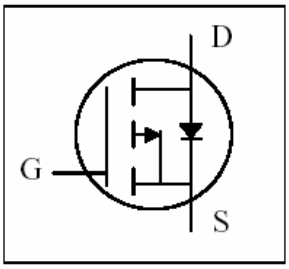
## Features

- Low On-Resistance
- Low Miller Charge
- Low Input Capacitance
- 100% EAS Guaranteed
- Green Device Available

## Package Dimensions




| REF. | Millimeter | | REF. | Millimeter | |
|---|---|---|---|---|---|
| | Min. | Max. | | Min. | Max. |
| A | 5.80 | 6.20 | M | 0.10 | 0.25 |
| B | 4.80 | 5.00 | H | 0.35 | 0.51 |
| C | 3.80 | 4.00 | L | 1.35 | 1.75 |
| D | 0° | 8° | J | 0.40 REF. | |
| E | 0.40 | 0.90 | K | 45° REF | |
| F | 0.19 | 0.25 | G | 1.27 TYP. | |

## Absolute Maximum Ratings

| Parameter | Symbol | Ratings | Unit |
|---|---|---|---|
| Drain-Source Voltage | $V_{DS}$ | -30 | V |
| Gate-Source Voltage | $V_{GS}$ | ±20 | V |
| Continuous Drain Current[1] | $I_D$ @$T_C$=25℃ | -15 | A |
| | $I_D$ @$T_C$=70℃ | -12 | A |
| Pulsed Drain Current[2] | $I_{DM}$ | -31 | A |
| Continuous Drain Current | $I_D$ @$T_A$=25℃ | -8.6 | A |
| | $I_D$ @$T_A$=70℃ | -6.9 | A |
| Single Pulse Avalanche Energy, L=0.1mH[3] | $E_{AS}$ | 105 | mJ |
| Single Pulse Avalanche Current, L=0.1mH[3] | $I_{AS}$ | -46 | A |
| Total Power Dissipation | $P_D$ @$T_C$=25℃ | 4.5 | W |
| | $P_D$ @$T_A$=25℃ | 1.5 | W |
| Operating Junction and Storage Temperature Range | $T_J$, $T_{STG}$ | -55 ~ +150 | ℃ |

## Thermal Data

| Parameter | Symbol | Conditions | Max. Value | Unit |
|---|---|---|---|---|
| Thermal Resistance Junction-ambient[2] | $R_{\theta JA}$ | Steady State | 85 | ℃/W |
| Thermal Resistance Junction-ambient[2] | $R_{\theta JC}$ | Steady State | 28 | ℃/W |

## Electrical Characteristics (Tj = 25℃ unless otherwise specified)

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Drain-Source Breakdown Voltage | $BV_{DSS}$ | -30 | - | - | V | $V_{GS}$=0, $I_D$=-250uA |
| Gate Threshold Voltage | $V_{GS(th)}$ | -1.0 | -1.65 | -2.5 | V | $V_{DS}$=$V_{GS}$, $I_D$=-250uA |
| Forward Transconductance | $g_{fs}$ | - | 24 | - | S | $V_{DS}$=-5V, $I_D$=-10A |
| Gate-Source Leakage Current | $I_{GSS}$ | - | - | ±100 | nA | $V_{GS}$= ±20V |
| Drain-Source Leakage Current(Tj=25℃) | $I_{DSS}$ | - | - | -1 | uA | $V_{DS}$=-24V, $V_{GS}$=0 |
| Static Drain-Source On-Resistance[2] | $R_{DS(ON)}$ | - | 10 | 12 | mΩ | $V_{GS}$=-10V, $I_D$=-12A |
| | | - | 16 | 20 | | $V_{GS}$=-4.5V, $I_D$=-8A |
| Total Gate Charge[2] | $Q_g$ | - | 21.5 | - | nC | $I_D$=-12A<br>$V_{DS}$=-15V<br>$V_{GS}$=-4.5V |
| Gate-Source Charge | $Q_{gs}$ | - | 8.5 | - | | |
| Gate-Drain ("Miller") Change | $Q_{gd}$ | - | 7 | - | | |
| Turn-on Delay Time[2] | $T_{d(on)}$ | - | 7.84 | - | ns | $V_{DD}$=-15V<br>$I_D$=-1A<br>$V_{GS}$=-10V<br>$R_G$=3.3Ω |
| Rise Time | $T_r$ | - | 72.2 | - | | |
| Turn-off Delay Time | $T_{d(off)}$ | - | 60.5 | - | | |
| Fall Time | $T_f$ | - | 23.9 | - | | |
| Input Capacitance | $C_{iss}$ | - | 2129 | - | pF | $V_{GS}$=0V<br>$V_{DS}$=-15V<br>f=1.0MHz |
| Output Capacitance | $C_{oss}$ | - | 298 | - | | |
| Reverse Transfer Capacitance | $C_{rss}$ | - | 227 | - | | |
| Gate Resistance | $R_g$ | - | 9 | - | Ω | f=1.0MHz |

## Guaranteed Avalanche Characteristics

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Single Pulse Avalanche Energy[5] | EAS | 54 | - | - | mJ | $V_{DD}$=-25V, L=0.1mH, $I_{AS}$=-33A |

## Source-Drain Diode

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Diode Forward Voltage | $V_{SD}$ | - | - | -1.0 | V | $I_S$=-1A, $V_{GS}$=0V, $T_J$=25℃ |
| Continuous Source Current[2,4] | $I_S$ | - | - | -15 | A | $V_G$=$V_D$=0V, Force Current |
| Pulsed Source Current[2,4] | $I_{SM}$ | - | - | -31 | A | |
| Reverse Recovery Time | $t_{rr}$ | - | 16.3 | - | ns | $I_F$=-6A, dI/dt=100A/μs,<br>$T_J$=25℃ |
| Reverse Recovery Charge | $Q_{rr}$ | - | 5.9 | - | nC | |

Notes: **1. The data tested by pulsed, pulse width ≦ 300us, duty cycle ≦ 2%.**

**2. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design. $R_{\theta JA}$ shown below for single device operation on FR-4 in still air.**

**3. The Min. value is 100% EAS tested guarantee.**

**4. The data is theoretically the same as ID and IDM, in real applications, should be limited by total power dissipation.**

## Typical Characteristics

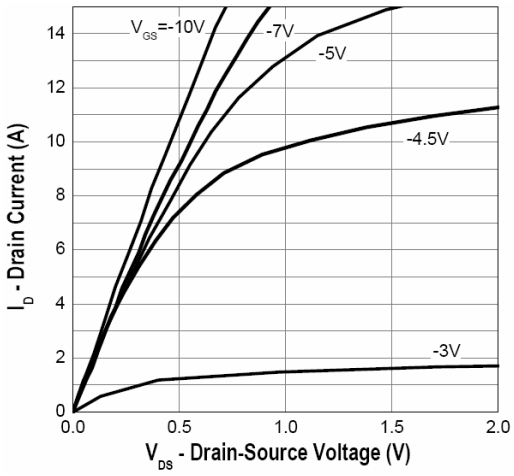



Fig.1 Typical Output Characteristics

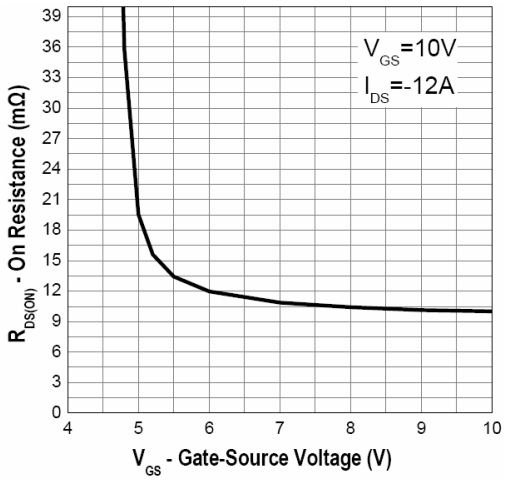



Fig.2 On-Resistance vs. G-S Voltage

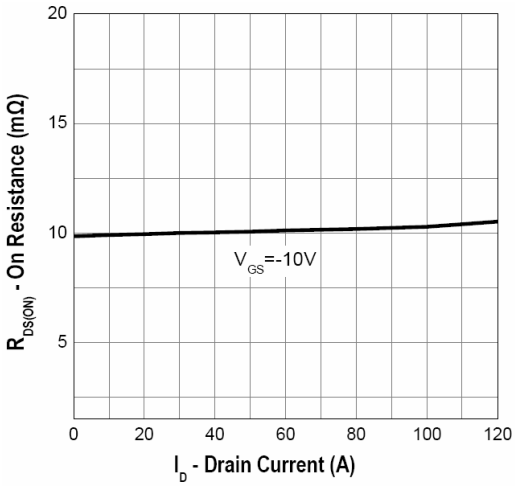



Fig.3 On-Resistance vs. Drain Current

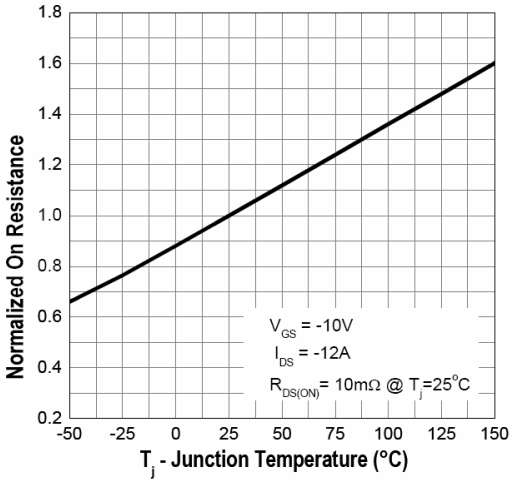



Fig.4 Normalized $R_{DSON}$ vs. $T_J$

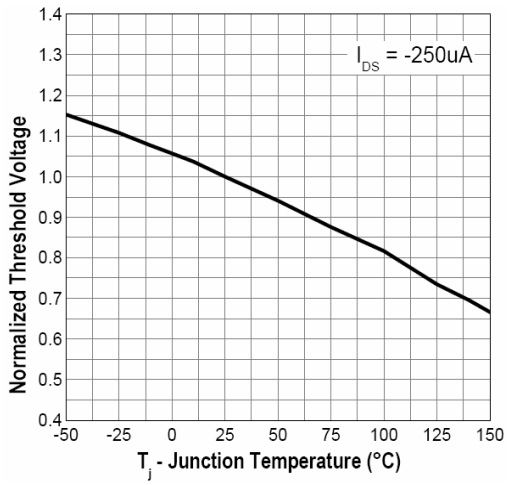



Fig.5 Normalized $V_{GS(th)}$ vs. $T_J$

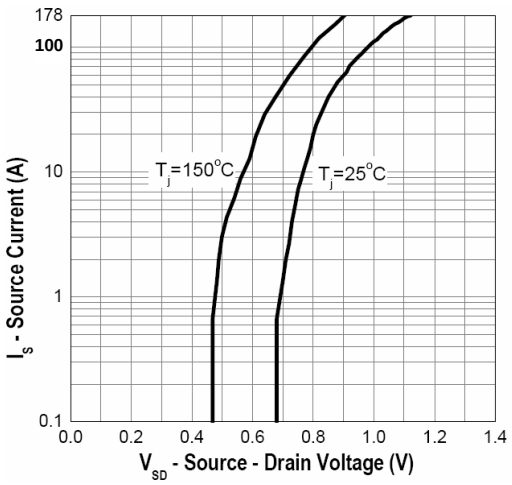



Fig.6 Forward Characteristics of Reverse

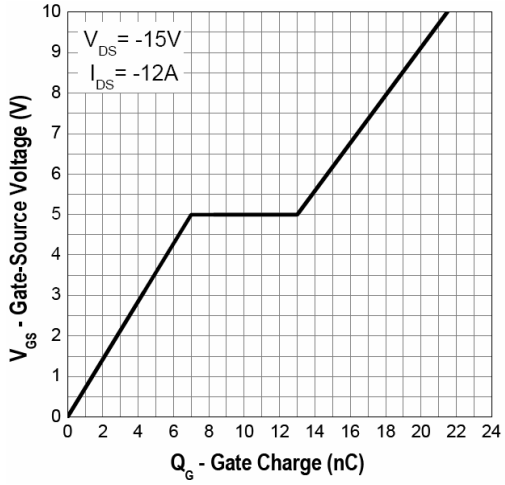



Fig.7 Gate Charge Characteristics

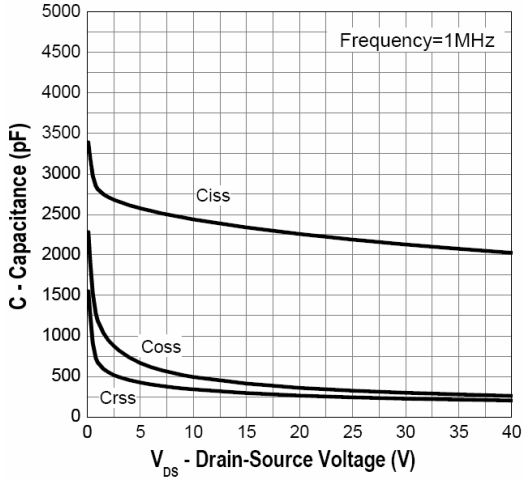



Fig.8 Capacitance Characteristics

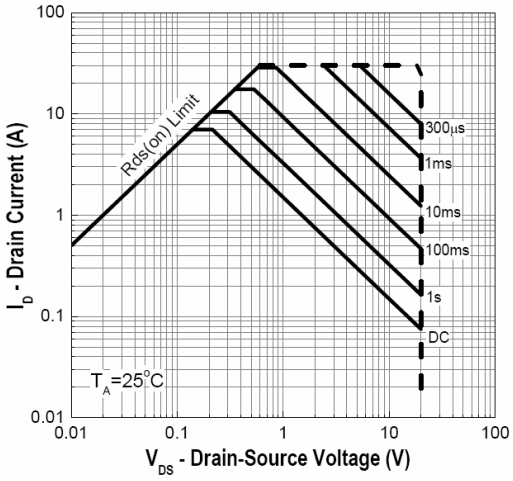



Fig.9 Safe Operating Area

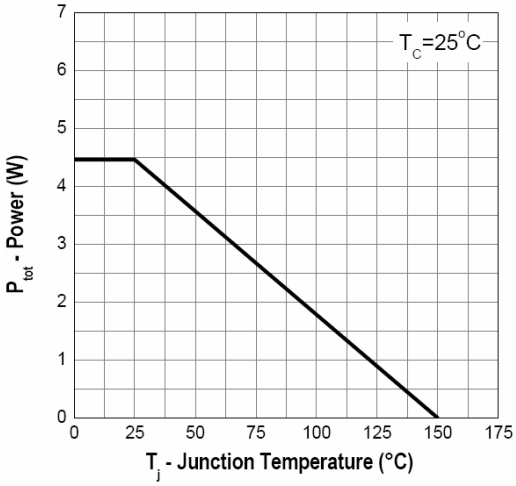



Fig.10 Power Dissipation

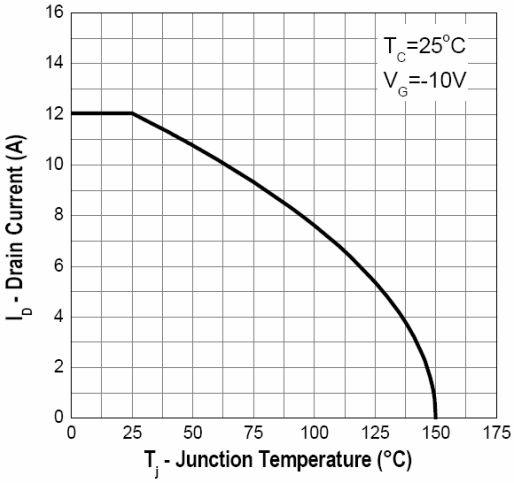



Fig.11 Drain Current vs. $T_J$

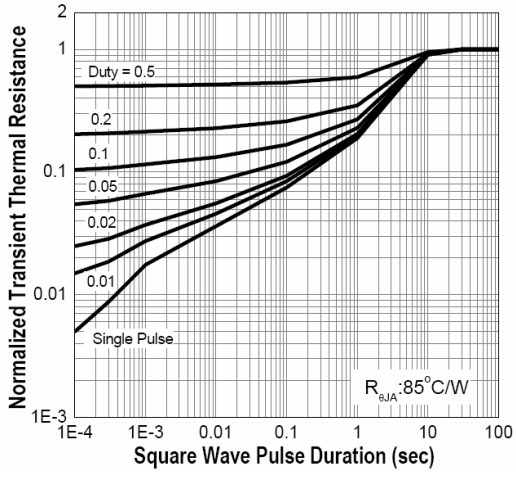



Fig.12 Transient Thermal Impedance